Review of Low Power and High Speed Implementation of 3-bit Flash Analog to Digital Converter

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ABSTRACT

In this paper, we present High speed and Low power implementation of 3-bit flash analog to digital converter. Analog to Digital converter is a device which converts continuous physical quantity to digital quantity. In the current CMOS technology power reduction is the foremost question at daily vitality. In advanced area, power utilization and low voltage form into wide component which is strenuous for disregard converters and high speed devices. In this paper by using diode based stacked power gating technique and low leakage stacked power gating technique a complete inquisition of 3-bit flash ADC circuit is proposed. These power gating method reduce the average power and the leakage current efficiently. The important criteria to effect the efficiency of data conversion systems are speed, resolution and power consumption. Simulation has been performed using cadence virtuoso tool at assorted power supply by 90nm technology to evaluate the power gating techniques.

KEY WORDS: Leakage Current, Stacked Power Gating Technique, 3-Bit Flash ADC, Power.

1. INTRODUCTION

This 3-bit flash ADC is a device which converts Analog form to digital form. This 3-bit flash ADC device otherwise known as parallel ADC. 2^N-1 comparators are used in N-bit converter ADC circuit, where N equals to 3. In this present scenario system-on-chip flourish more; so signal processing component utilization is a most important factor. It is having high speed in GIGA sample and power consumption in mW. In this 3-bit flash ADC comparator plays a prominent role. To compare two signals a comparator is a needed device in ADC. In this paper differential based comparator is used which is having high frequency.

Encoder is a part which is used in flash ADC, it locates besides the comparator this sleep transistor is placed in between circuit ground and actual ground. Power utilization, resolution and speed can be the important factor for some data conversion system efficiency. This complete inspect has simulated in cadence tool in GPDK 90nm CMOS technology using supply voltage as 1.2V.

Background:

Explaining the blocks present in 3-bit flash ADC:

Comparator: There are different types of comparators. Some of them are discussed below. Showing different comparators in the below table with respective to their supply voltage and power consumption.

Table.1. Different types of comparator

Comparators	Supply voltage	Power consumption
OPAMP based	1.2V	52.80 mw
Differential comparator	1.2V	49.94mw
Double tail	1.2V	0.006mw
Dynamic latched	1.2V	0.003mw
Current mode saturation	1.2V	0.6mw
Current mode subthreshold	1.2V	114.2mw

In this paper used differential comparator. Comparator is a device which compares two input signals and gives output as digital signal. It have two analog input terminals V+ and V- and output Vo.

$$V0 = \begin{cases} 1, \text{ IF } V+ > V- \\ 0, \text{ IF } V+ < V- \end{cases}$$

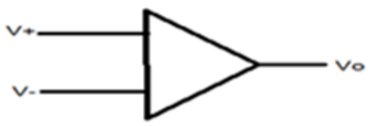

Figure.1. Symbol for comparator

Comparator was designed with input DC voltage 0.6V and VDD as 1.2V. This comparator will be applicable up to 6GHZ. Done outputs with transient and DC analysis.

Encoder: Encoder can be designed in many ways using gates. There are different types of Encoder. Some of them are explained below. Showing different Encoders in the below table with respective to their delay, power, and their advantages.

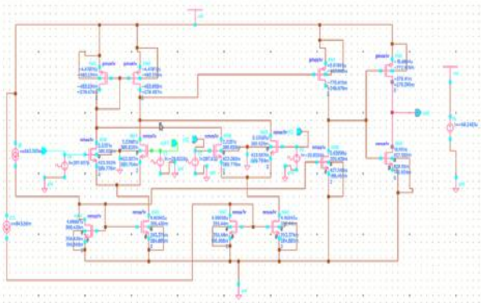

Figure.2. Schematic of comparator

Table.2. Comparison of different Encoder

	Rom based encoder	**Wallace tree encoder**	**Fat tree encoder**	**Mux based encoder**
Delay (ns)	0.1346	4.05	0.09343	0.1325
Power (u wat)	431.8	8.27	0.1104	0.0442
Advantage	Contain an in encoder portion and thermometer 2:1 hot code then into binary, simple desing	Offer global error correction consists of full adder in encoder portion	Thermometer 2:1 to In conde then into binary, implement using XOR and XNOR in encoder portion. Faster than ROM based	High speed, low power consumption, low circuit complexity
Disadvantage	Slow speed, larger power consumption, bubble error	Latency problem, high routing complexity	Slow and more consumption	

Now here we can see that Encoder also is current mode which is basically to attain high speed in this complete work we have simulated three different type of Encoder and on the basis of that we can say that MUX based Encoder is fastest and less power consuming and in MUX based Encoder we can simulate for three different topology which are as follows

- Implementation of 2:1 multiplexer using basic gate
- Implementation of 2:1 multiplexer using transmission gate
- Implementation of 2:1 multiplexer using current mode logic multiplexer.

In this paper we used 2:1 multiplexer using basic gate. The schematic of the 2:1 multiplexer using basic gate can be designed by using AND, OR and NOT gates .Whereas 2 AND gates, 1 OR gate and 1 NOT gate. Hence schematic was shown below.

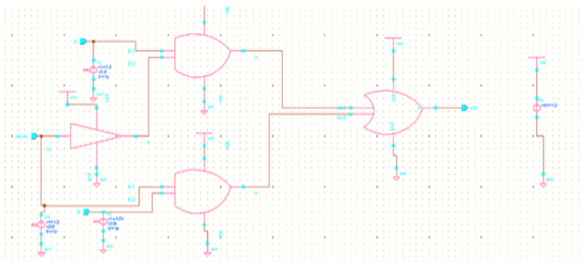

Figure.3. 2:1 MUX using basic gates

First designing AND, NOR and NOT gates using CMOS technology in the gpdk90nm and creating symbol for that and forming 2:1MUX. This MUX was designed with VDD=1.2, DC voltage as 1.2. MUX formula shown below.

$$Z = (A.S) + (B.S) \quad \begin{cases} \text{Where } S=0, & Z=A \\ S=1, & Z=B \end{cases}$$

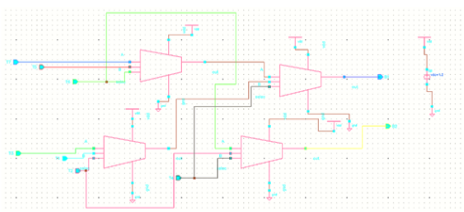

Figure.4. 8:3 Encoder using MUX

8:3 Encoder is designed with MUX. Using stimuli procedure and giving VDD as 1.2V and done simulation in cadence and creating symbol for the 8:3 Encoder.

BIT FLASH ADC: Different types of flash ADC are discussed below:

Table.3. Comparison of different ADC

	Flash ADC	SAR ADC	Pipeline ADC	Integrating ADC	Sigma delta ADC
Advantage	High speed in giga sample	Medium resolution 8-16 bit, speed in mega sample, low power and small size, less expensive and determine one bit at a time	Resolution between 8-14 bits, speed 100Mbps, low power consumption than flash	Use in monitoring of DC signal, in industrial and DC signal, high resolution around 16bit, less expensive, less power consumption, good noise performance, speed 100Mbps	High resolution 12-24 bit, lower bandwidth
Disadvantage	Power consumption in milli watt	Speed less 5 Mbps	Latency		Not applicable for multichannel, require filter to remove noise

Flash ADC Architecture:

Flash ADC: Flash ADC architecture is shown below which is designed and implemented in gpdk90 nm CMOS technology. 3-bit flash ADC is a circuit which consists of 2^N-1 comparators, where N=3. 2^3 -1 = 7 so using 7 comparators.

Table.4. Comparison of different ADC

Conversion method	N bits 2^N-1 comparators	Binary search algorithm, internal circuitry runs higher speed	Unknown input voltage is integrated and value compared against known reference value	Small parallel structure, each stage works on one to a few bits	Oversampling ADC, 5-HZ to 60 HZ rejection programmable data output
Encoding method	Thermometer code encoding	Successive approximation	Analog integration	Digital correction logic	Over sampling modulator, digital decimation filter
Disadvantages	Sparkle codes, met stability, high power consumption, large size, expensive	Speed limited to 5Mbps may require anti-aliasing filter	Slow conversion rate. High precision external components required to achieve accuracy	Parallelism increases throughput at the expense of power and latency	Higher order (4^{th} order or higher) – multibit ADC and multibit feedback DAC
Conversion time	Conversion time does not change with increased resolution	Increases linearly with increased resolution	Conversion time doubles with every bit increase in resolution	Increase linearly with increased resolution	Trade-off between data output rate and noise free resolution
Resolution	Component matching typically limits resolution to 8 bits	Component matching requirements double with every bit increases in resolution	Component matching does not increase with increase in resolution	Component matching requirements double with every bit increase in resolution	Component matching requirements double with every bit increase in resolution
Size	2^N-1 comparators, die size and power increases exponentially with resolution	Die increases linearly with increase in resolution	Core die size will not materially change with increase in resolution	Die increases linear with increase in resolution	Core die size will not materially change with increase in resolution

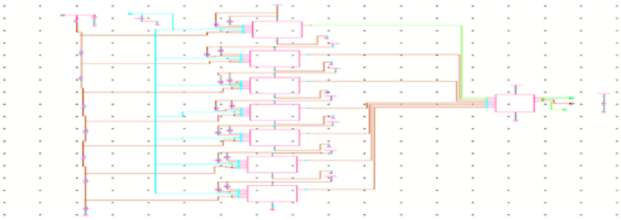

Figure.5. Schematic of 3-bit flash ADC

Stacked power gating technique: Below figure shows the stacked power gating technique used in flash ADC. In this technique sleep transistors are used, by using these transistors leakage current may reduce. Here ST1 and ST2 are the sleep transistors. ST1 and ST2 will be off in standby mode; hence in this condition leakage current may reduce.

While doing simulation we will observe 3 modes.

Active mode: Both ST1 and ST2 will be staying in ON condition i.e., sleep transistor remains at logic 1. In this mode both transistors may have low resistance.

Voltage across C1 = VC1 (active mode) =V (R1ON) + (R2ON)

Voltage across C2 = VC2 (active mode) =V (R2ON) =0V

Standby mode: Both ST1 & ST2 are off on standby mode and both offers high resistance. Capacitance C1 charges up to voltage V1 and capacitance C2 charges up to voltage V2. So, VC1 (Standby mode) = V1, VC2 (Standby mode) = V2

Sleep to active mode transition: In this sleep transistor will be off. Control signal will be in on condition. The parameters T1 and capacitances C2 will keep to particular value that is based on following factors: Minimum ground bounce noise, Minimum leakage current.

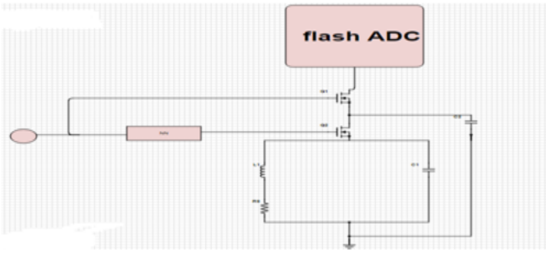

Figure.6. Schematic of stacked power gating

Diode based stacked power gating technique:

- Transistor M1 and M2 are sleep transistors. For less leakage current these transistors use high threshold voltage.
- To make sleep transistor M1 functioning as diode during mode transition T1 is used as control transistor.

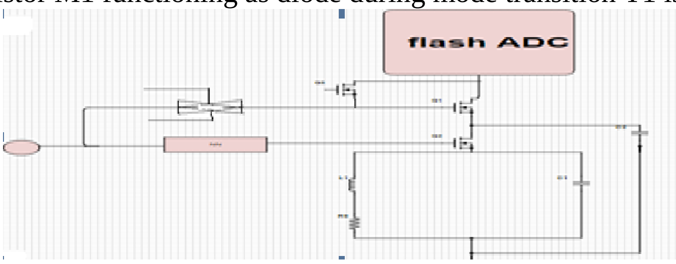

Figure.7. Diode based power gating technique

Modification of this project: In the given paper the circuit will be applicable up to 1GHZ hence by modifying the comparator the circuit will be applicable more than 1GHZ. Hence these type of circuits may use in different applications.

Modified comparator is shown below;

Design parameters of the circuit is Technology library: gpdk 90nm, Supply voltage: 1.2V, Length: 100nm, Width: according to their sizing

2. CONCLUSION

Flash ADC topology is nothing but fastest ADC topology, by using higher bandwidth flash ADC will increase speed and power dissipation is increases exponentially. If circuit contains high speed and power dissipation can use in different applications, hence this project used in Ultra-Wide Band application.

Hence shown Designing and implementing the circuit of 3-bit Analog to Digital, whereas by using power gating technique to the flash ADC for reducing leakage current and average power. Designing and implementing the circuit of 3-bit Analog to Digital by using power gating technique to the flash ADC for reducing leakage current and average power. Hence these techniques are going to design in gpdk45 nm technology.

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